REMARKS

The Examiner contends that the title of the invention is not descriptive. Applicants disagree and assert that the title of the invention is clearly descriptive of the invention as claimed, as would be understood by one of ordinary skill in the art. Applicants request that if the Examiner feels the title is not descriptive, that he provide specific remarks indicating why he feels it is not descriptive.

Claims 1, 5-6, 14, 17-21, 25 and 27 have been amended. No claims have been added or cancelled. Therefore claims 1-31 remain pending in the application. Reconsideration is respectfully requested in light of the following remarks.

Section 102(b) Rejection:

The Examiner rejected claims 1-3, 5-6, 8-22, 24-25 and 27-31 under 35 U.S.C. § 102(b) as being anticipated by Webb et al. (U.S. Patent 6,360,314) (hereinafter "Webb"). Applicants traverse this rejection for at least the following reasons.

Regarding claim 1, contrary to the Examiner's assertion, Webb fails to teach or suggest *a load store unit configured to store information associated with load and store operations dispatched by the dispatch unit, wherein the load store unit includes a STLF (Store-to-Load Forwarding) buffer, wherein STLF buffer includes a plurality of entries; wherein the load store unit is configured to generate an index dependent on at least a portion of an address of a load operation, to use the index to select one of the plurality of entries*. First, Webb does not disclose a load store unit configured to store information associate with load and store operations, nor including a Store-to-Load Forwarding (STLF) buffer. The Examiner refers to FIG. 4, including buffer 428 and queue 426 as teaching these limitations. However, FIG. 4 clearly illustrates that store data buffer 428 and store queue 426 are components of data cache subsystem 420, and not load/store unit 418.

Further regarding claim 1, Webb does not disclose the load store unit generating an index and using the index to select one of the entries in the STLF buffer. The Examiner cites column 5, lines 5-8 and 19-22, as teaching these limitations. However, there is nothing in these citations that teaches that the load store unit, or any other apparatus, is configured to **generate** an index. They only describe the use of an index. Furthermore, the index referred to in these citations is not an index into a STLF buffer, or to Webb's store queue 426 and store data buffer 428, which the Examiner equates with Applicants' STLF buffer. Instead, these citations describe indexing into dcache unit 430, and its components (tag store 432 and data store 434.) Therefore, Webb clearly does not teach these limitations of Applicants' claim 1.

As the Examiner is no doubt aware, anticipation requires the presence in a single prior art reference disclosure of each and every limitation of the claimed invention, arranged as in the claim. M.P.E.P 2131; *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The identical invention must be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). As discussed above, Webb fails to disclose *a load store unit configured to store information associated with load and store operations dispatched by the dispatch unit, wherein the load store unit includes a STLF (Store-to-Load Forwarding) buffer, wherein STLF buffer includes a plurality of entries; wherein the load store unit is configured to generate an index dependent on at least a portion of an address of a load operation, to use the index to select one of the plurality of entries*. Therefore, Webb cannot be said to anticipate claim 1.

For at least the reasons above, the rejection of claim 1 is not supported by the cited art and removal thereof is respectfully requested. Claim 14 includes limitations similar to claim 1, and so the arguments presented above apply with equal force to this claim, as well.

Regarding independent claim 20, contrary to the Examiner's assertion, Webb fails to teach or suggest *generating an index corresponding to the address* and *using the index*

to select an entry from a plurality of entries included in a STLF (Store-to-Load Forwarding) buffer. The Examiner cites column 5, lines 5-22 as teaching this limitation. However, as discussed above regarding claim 1, Webb discloses neither generating an index, nor using an index to select an entry in a STLF buffer, as recited in claim 20.

For at least the reasons above, the rejection of claim 20 is not supported by the cited art and removal thereof is respectfully requested.

Regarding claim 5, contrary to the Examiner's assertion, Webb fails to teach or suggest *the load store unit is configured to select which one of the plurality of entries to allocate to a store operation by generating an additional index dependent on at least a portion of an address of the store operation.* The Examiner again cites column 5, lines 5-8 and 19-23 as teaching this limitation. However, as discussed above, there is nothing in Webb that teaches the load store unit is configured to generate an index at all, much less two indices, and these citations describe indexing into dcache 430, not into a STLF buffer, or store queue 426 and store data buffer 428.

For at least the reasons above, the rejection of claim 5 is not supported by the cited art and removal thereof is respectfully requested. Claims 16 and 24 include limitations similar to claim 5, and so the arguments presented above apply with equal force to these claims, as well. Applicants note that the Examiner rejected claim 22 along with claim 5 in his remarks. Applicants assume that this was a typographical error, as claim 24 (and not claim 22) recites limitations similar to those in claim 5.

Regarding claim 6, contrary to the Examiner's assertion, Webb fails to teach or suggest *the load store unit is configured to generate the additional index dependent on both the at least a portion of the address of the store operation and a number of bytes of data operated on by the store operation, and wherein the load store unit is configured to generate the index dependent on both the at least a portion of the address of the load operation and a number of bytes of data operated on by the load operation.* The Examiner again cites column 5, lines 5-8 and 19-23, as teaching that the load store unit is

configured to generate this index. However, as discussed above regarding claim 5, Webb does not teach this limitation. The Examiner cites column 6, lines 51-59, as teaching that the index is generated dependent on the number of bytes of data operated on by the store operation. While this citation describes a comparison between the size field 48 of a store queue entry and the size information of an issuing load, it does not describe generating an index into a STLF buffer dependent on this information. The Examiner asserts that the "data size is used as an index to determine if a TRAP signal is to be generated...". However, as would be understood by one of ordinary skill in the art, using a comparison of two data size values to generate a signal is clearly not the same as generating an index dependent on a data size value.

For at least the reasons above, the rejection of claim 6 is not supported by the cited art and removal thereof is respectfully requested. Claims 17 and 25 include limitations similar to claim 6, and so the arguments presented above apply with equal force to these claims, as well.

Regarding claim 8, contrary to the Examiner's assertion, Webb fails to teach or suggest *the additional index comprises a portion of the address targeted by the store operation*. The Examiner again cites column 5, lines 19-22, as teaching this limitation. However, this citation describes indexing (using a portion of an address) into dcache unit 430, not into a STLF buffer, or into Webb's store queue 426 and store data buffer 428. Using an address to index into dcache unit 430 teaches nothing about the composition of the additional index (for selecting an entry in the STLF buffer) referred to in Applicants' claim 8.

For at least the reasons above, the rejection of claim 8 is not supported by the cited art and removal thereof is respectfully requested. Claim 27 includes limitations similar to claim 8, and so the arguments presented above apply with equal force to this claim, as well.

Regarding claim 9, contrary to the Examiner's assertion, Webb fails to teach or suggest *the load store unit further comprises a STLF checker configured to verify operation of the STLF buffer*. The Examiner cites column 7, lines 5-8, as teaching this limitation, and asserts that Webb's invention contains a unit which verifies operation, specified as the apparatus disclosed in column 7, lines 5-8. However, the Examiner's citation describes only that, "The present invention provides a methodology and apparatus for determining which of the multiple stores should be used in bypassing the dcache unit 430." This does not describe a unit *configured to verify operation of the STLF buffer*, as recited in claim 9, but describes only one of the operations of "an apparatus" that has nothing to do with verifying operation of the STLF buffer. This citation also does not describe that this unit is part of the load store unit (e.g., Webb's load/store unit 418), as recited in claim 9.

For at least the reasons above, the rejection of claim 9 is not supported by the cited art and removal thereof is respectfully requested. Claim 18 includes limitations similar to claim 9, and so the arguments presented above apply with equal force to this claim, as well.

Regarding claim 11, contrary to the Examiner's assertion, Webb fails to teach or suggest *the STLF checker is configured to replay the load operation if the STLF checker identifies incorrect operation of the STLF buffer*. The Examiner cites column 1, lines 34-38 as teaching this limitation and asserts that if a load operation does not result in data being provided from the cache, the memory load is replayed to the main memory. This is incorrect. First, this citation teaches nothing about replaying a load operation. It merely describes that the data for a load is retrieved from main memory, instead of from the cache, if it is not found in the cache. Furthermore, this citation has nothing to do with a STLF checker identifying incorrect operation of the STLF buffer. In fact, this citation has nothing to do with the STLF buffer at all. Instead, as stated above, this citation describes only that if data is not found in the cache, it is retrieved from main memory.

For at least the following reasons, the rejection of claim 11 is not supported by the cited art and removal thereof is respectfully requested. Claims 19 and 29 include limitations similar to claim 11, and so the arguments presented above apply with equal force to these claims, as well.

Regarding claim 12, contrary to the Examiner's assertion, Webb fails to teach or suggest *the STLF checker is configured to replay one or more additional operations that are dependent on the load operation if the STLF checker detects incorrect operation of the STLF buffer.* The Examiner cites column 7, lines 63-65, as teaching this limitation and asserts that after the in-flight instructions are killed they must inherently be reissued. The Examiner contends that if the instructions are not reissued, the program may produce undesired output or simply cease operation. The Examiner's citation describes that a TRAP signal 454 is provided by store queue 426 to indicate that the bypass mechanism did not provide data when it should have and therefore, the in-flight instructions should be killed. Applicants assert that the system of Webb could respond to the TRAP signal in any number of ways to produce the correct output or prevent the program from ceasing operation. There is nothing in Webb that teaches or suggests that the response to this signal is to *replay one or more additional operations that are dependent on the load operation*, as recited in claim 12. As there is no detailed description of the scheduling of instructions in Webb, or of any **replay** mechanism at all, the Examiner's assertion that one or more additional operations that are dependent on the load operation must be replayed is mere speculation, not a necessary condition of operation.

Applicants remind the Examiner that, "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is **necessarily present** in the things described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPA2d 1949, 1950-51 (Fed. Cir. 1999) (emphasis added). As discussed above, the system of Webb would not necessarily need to *replay one or more additional operations that are*

dependent on the load operation if the STLF checker detects incorrect operation of the STLF buffer.

For at least the reasons above, the rejection of claim 12 is not supported by the cited art and removal thereof is respectfully requested. Claim 30 includes limitations similar to claim 12, and so the arguments presented above apply with equal force to this claim, as well.

Regarding claim 13, contrary to the Examiner's assertion, Webb fails to teach or suggest *the load store unit is configured to identify the result of the load operation as a speculative value in response to forwarding the data in the one of the plurality of entries included in the STLF buffer as the result of the load operation; wherein if the STLF checker verifies that the STLF buffer operated correctly for the load operation, the load store unit is configured to indicate that the result of the load operation is not speculative.* The Examiner asserts that while a load operation is pending in the store buffer/queue (while the address lookup is operating) the operation is speculative, as no data has yet been forwarded. The Examiner further asserts that when the index has been calculated, and the apparatus determines the entry to be the youngest and of the correct size, the data is forwarded and is then no longer considered speculative. The Examiner is incorrect. First, claim 13 clearly recites that the load store unit identifies the result of the load operation as speculative in response to forwarding the data in the one of the plurality of entries included in the STLF buffer as the result of the load operation, that is, the result is identified as speculative **after the load operation and after the data has been forwarded**, not while the load operation is pending, as the Examiner asserts. The Examiner is not describing a form of speculation, as recited in claim 13 and as would be understood by one of ordinary skill in the art, nor does Webb disclose this speculation. Instead, rather than describing a case in which the results of the load operation are speculative, the Examiner appears to be describing that the load operation itself is speculative, which has nothing to do with Applicants' claims.

Further regarding claim 13, Webb does not disclose that the load store unit, or any other apparatus, is configured to identify the result of the load operation as a speculative

value. Even if the Examiner's assertions regarding speculation were correct, which they are not, Webb does not disclose providing any indication that the result of the load operation is speculative or not speculative, as recited in claim 13.

For at least the reasons above, the rejection of claim 13 is not supported by the cited art and removal thereof is respectfully requested. Claim 31 includes limitations similar to claim 13, and so the arguments presented above apply with equal force to this claim, as well.

Applicants also assert that numerous other ones of the dependent claims recite further distinctions over the cited art. However, since the rejection has been shown to be unsupported for the independent claims, a further discussion of the dependent claims is not necessary at this time.

Section 103(a) Rejections:

The Examiner rejected claims 4 and 23 under 35 U.S.C. § 103(a) as being unpatentable over Webb, and claims 7 and 26 as being unpatentable over Webb in view of Hennessy ("Computer Organization and Design"). Applicants traverse these rejections for at least the reasons given above in regard to the claims from which claims 4, 7, 23 and 26 depend. Applicants also reserve the right to present additional arguments.

OIPE IAP57
APR 17 2006
PATENT & TRADEMARK OFFICE

CONCLUSION

Applicants submit the application is in condition for allowance, and prompt notice to that effect is respectfully requested.

If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above-referenced application from becoming abandoned, Applicants hereby petition for such an extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-89400/RCK.

Also enclosed herewith are the following items:

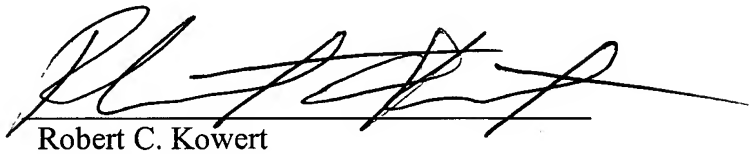
☒ Return Receipt Postcard

☐ Petition for Extension of Time

☐ Notice of Change of Address

☐ Other:

Respectfully submitted,



Robert C. Kowert
Reg. No. 39,255
ATTORNEY FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8850

Date: April 12, 2006